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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/707,867	01/20/2004	YAO-CHI WANG	11870-US-PA	1866

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JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER	
NGUYEN, LINH V	
ART UNIT	**PAPER NUMBER**
2819	

DATE MAILED: 09/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/707,867	WANG, YAO-CHI	
	Examiner	Art Unit	
	Linh V Nguyen	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledge of papers submitted under 35 U.S.C 119(a)-(d), which papers have been placed of record in the file.

Specification

2. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1 – 4, and 7 – 9 are rejected under 35 U.S.C. 102(b) as being anticipated by Kusumoto et al. U.S. Patent No. 6,025,794.

Regarding claim 1, Fig. 24 of Kusumoto et al. discloses a threshold voltage control circuit, comprising: a first capacitor (C0), having a first terminal and a second terminal (top and bottom terminals of capacitor C0), wherein said first terminal (bottom

terminal of capacitor 50) is coupled to a first voltage level (Ground); a clock generator (Col. 22 lines 50 - 53) for generating a plurality of clock signals (Fig. 25) and a switching capacitor network (248, 249), coupled to said second terminal of said first capacitor (Top terminal of capacitor C0), wherein the switching capacitor network receives an analog signal (241, Col. 18 lines 43 - 45) and said clock signals, stores a portion of charges of said analog signal (Col. 18 lines 42 - 45), and outputs said portion of charges according to said clock signals (Col. 18 lines 45 - 48), and generates a threshold voltage associated with said first capacitor (Col. 18 lines 51 - 52).

Regarding claim 2, wherein said switching capacitor network comprises a plurality of sensor control switches (248, 249), wherein one of controlled by said clock said sensor control switches is signals for turning on/off (Fig. 25), said sensor control switches (248, 249) are series-connected to for a series structure (248, 249) having a first terminal and a second terminal (left and right terminals of transistor 248), said first terminal (left terminal of 248) of said series structure receiving said analog signal (241) and said second terminal (right terminal of 248) of series structure being coupled to said second terminal of said first capacitor (top terminal of C0) to output said threshold voltage, and at least a second capacitor (C1), having a first terminal (top terminal of C1) and a second terminal (bottom terminal of C1), wherein said first terminal of said second capacitor (top terminal of C1) is coupled to a node (243) connected to two adjacent sensor control switches (248, 249) in said series structure, said second terminal of said second capacitor is coupled to a second voltage level (Ground Level).

Regarding claim 3, wherein said of clock signals have a same frequency with different phases respectively (Fig. 25 discloses clocks for switches 248, 249 having the same frequency with different on/off phases).

Regarding claim 4, wherein said pluralities of clock signals do not overlap (Fig. 25 discloses the ON clock signal 248 does not overlap the On Clock signal 249).

Regarding claim 7, wherein said circuit applies to a frequency-shift keying communication system (this claim is intend of use only, since it has been held that a recitation with respect to the manner in which claim apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claim structural limitations. *Ex parte Masham,* 2 USPQ2d 1647 (1987)).

Regarding claim 8, wherein said circuit applies to an amplitude-shift keying communication system (this claim is intend of use only, since it has been held that a recitation with respect to the manner in which claim apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claim structural limitations. *Ex parte Masham,* 2 USPQ2d 1647 (1987)).

Regarding claim 9, wherein said circuit applies to an on/off keying communication system (this claim is intend of use only, since it has been held that a recitation with respect to the manner in which claim apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claim structural limitations. *Ex parte Masham,* 2 USPQ2d 1647 (1987)).

5. Claims 10, 11, and 16 - 19 are rejected under 35 U.S.C. 102(b) as being anticipated by Zhou et al. U.S. Patent No. 6,124,819.

Regarding claim 10, Fig. 6 of Zhou et al. discloses an analog-to-digital converter, comprising: a first capacitor (50), having a first terminal and a second terminal (top and bottom terminals of capacitor 50), wherein said first terminal (bottom terminal of capacitor 50) is coupled to a first voltage level (V+); a clock generator (Fig. 7) for generating a plurality of clock signals (Fig. 7 (Φ_{on} --- Φ_{Ref})) and a switching capacitor network (MOS transistors of 75, 80, 84, 74), coupled to said second terminal of said first capacitor (Top terminal of capacitor 50), wherein the switching capacitor network receives an analog signal (Vs, VR, Vref) and said clock signals (Φ_R, Φ_S ,Φ_{Ref}) stores a portion of charges of said analog signal (Col. 8 lines 11 – 13), and outputs said portion of charges according to said clock signals (Col. 8 lines 17 - 18), and generates a threshold voltage associated with said first capacitor (Col. 8 lines 19 - 20); and a comparator (62), for comparing said threshold voltage with said analog signal (Col. 8 lines 38 – 39) and outputting a digital signal (Col. 7 lines 49 – 51).

Regarding claim 11, wherein said switching capacitor network comprises a plurality of sensor control switches (MOS transistors of 75, 80, 84, 74), wherein one of controlled by said clock said sensor control switches is signals for turning on/off (Col. 8 lines 24 – 28), said sensor control switches (80, 74) are series-connected to for a series structure having a first terminal and a second terminal (left and right terminals of transistor 80), said first terminal (left terminal of 80) of said series structure receiving said analog signal (VS) and said second terminal (right terminal of 80) of series

structure being coupled to said second terminal of said first capacitor (50) to output said threshold voltage, and at least a second capacitor (52), having a first terminal (top terminal of 52) and a second terminal (bottom terminal of 52), wherein said first terminal of said second capacitor (top terminal of 52) is coupled to a node (right terminal of 74) connected to two adjacent sensor control switches (80, 74) in said series structure, said second terminal of said second capacitor is coupled to a second voltage level (V+).

Regarding claim 16, wherein said circuit applies to a frequency-shift keying communication system (this claim is intend of use only, since it has been held that a recitation with respect to the manner in which claim apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claim structural limitations. *Ex parte Masham,* 2 USPQ2d 1647 (1987)).

Regarding claim 17, wherein said circuit applies to an amplitude-shift keying communication system (this claim is intend of use only, since it has been held that a recitation with respect to the manner in which claim apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claim structural limitations. *Ex parte Masham,* 2 USPQ2d 1647 (1987)).

Regarding claim 18, wherein said circuit applies to an on/off keying communication system (this claim is intend of use only, since it has been held that a recitation with respect to the manner in which claim apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claim structural limitations. *Ex parte Masham,* 2 USPQ2d 1647 (1987)).

Regarding claim 19, Fig. 6 of Zhou et al. discloses a method for converter an analog signal to a digital signal, comprising: providing a first capacitor (50) and a plurality of clock signals (Fig. 7 (Φ_{on} --- Φ_{Ref})); storing a portion of charges of an analog signal according to said clock signals (Col. 8 lines 11 – 13), generating a threshold voltage according to said clock signals (Col. 8 lines 13 - 21) based on said portion of charges associated with said first capacitor (Col. 8 lines 13 - 21); and comparing (62) said threshold voltage with said analog signal (Col. 8 lines 38 – 39) in order to output a digital signal (Col. 7 lines 49 – 51).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kusumoto et al. as applied to claim as applied to claim 4 above, and further in view of Zhou et al. as applied to claim 10 above.

Regarding claim 5, Fig. 24 of Kusumoto et al. as applied to claim 4 above disclose almost every aspect of applicant's claimed invention, however wherein the plurality of sensor control switches (248, 249) of Kusumoto et al. are silent to MOSFETS.

Fig. 6 of Zhou et al. as applied to claim 10 above teaches a switching capacitor networks (150, 152) having sensor control switches are MOSFETS (180, 174).

Kusumoto et al. and Zhou et al. are common subject matter for Analog to Digital converter with switching capacitors network. Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the MOSFET switches taught by Zhou et al. into the switches of Kusumoto et al. because CMOS is well suited for Analog to Digital converter and providing minimal chip area (Zhou et al. Col. 4 lines 16 – 19).

Regarding claim 6, modified Kusumoto as applied to claim 5 above, further discloses wherein said first voltage level and said second voltage level are DC voltage levels (Kusumoto's Fig. 24 discloses the first capacitor C0 coupled to a first DC voltage level "Ground", and the second capacitor C1 coupled to a second DC voltage level "Ground").

8. Claims 12 – 15 and 20 rejected under 35 U.S.C. 103(a) as being unpatentable over Zhou et al. as applied to claim as applied to claim 11 above, and further in view of Kusumoto et al. as applied to claim 3 above.

Regarding claim 12, Zhou et al. as applied to claim 11 above, further discloses the clock signals have different ON phases for each of the clock signals respectively (Zhou et al. Fig. 7), however Zhou et al. fails to teach the clocks have a same frequency.

Fig. 25 of Kusumoto et al. as applied to claim 3 above, discloses wherein said of clock signals have a same frequency with different phases respectively (Fig. 25 discloses clocks for switches 248, 249 having the same frequency with different on/off phases).

Kusumoto et al. and Zhou et al. are common subject matter for Analog to Digital converter with plurality clocks signal for controlling switching capacitors network. Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the clocks having the same frequency taught by Kusumoto et al. into the clocks of Zhou et al. for the purpose of improving current consumption and settling time of signal transferring circuit (Kusumoto et al. Col. 42 – 62).

Regarding claim 13, modified Zhou et al. as applied to claim 12 above, and further discloses wherein said clock signals do not overlap (Zhou et al., Col. 12 lines 64 – 65 of Zhou et al.).

Regarding claim 14, Zhou et al. as applied to claim 13 above, further discloses wherein switches are MOSFETS said sensor control (Zhou, Fig. 6 [176, 180, 184, 174]).

Regarding claims 15, Fig. 6 of Zhou et al. as applied to claim 14 above, and further discloses wherein said first voltage level (first branch of V+) and said second voltage level (second branch of V+) are DC voltage levels (Col. 8 line 52 discloses 2 volts of V+).

Regarding claim 20, Fig. 6 of Zhou et al. as applied to claim 19 above, and further discloses wherein said clock signals comprises a first clock signal (Φ_S) and a

second clock signal (Φ_{IS}) said first and second clock signals not overlapping (Col. 12 lines 64), and said step of generating said threshold voltage further comprising: providing a second capacitor (52), conducting said analog signal to said second capacitor according to said first clock signal (Φ_S) to store said portion of charges of said analog signal in said second capacitor (Col. 8 lines 24 – 26), and conducting said first capacitor and said second capacitor in response to said second clock signal (Col. 8 lines 26 – 28) in order to generate said threshold voltage based on said portion of charges of said analog signal associated with said first capacitor (Col. 8 lines 28 – 31), however Zhou et al. fails to disclose the clocks have a same frequency.

Kusumoto et al. as applied to claim 3 above discloses wherein said of clock signals have a same frequency with different phases respectively (Fig. 25 discloses clocks for switches 248, 249 having the same frequency with different on/off phases).

Zhou et al. and Kusumoto et al. are common subject matter for Analog to Digital converter with plurality clocks signal for controlling switching capacitors network. Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the clocks having the same frequency taught by Kusumoto et al. into the clocks of Zhou et al. for the purpose of improving current consumption and settling time of signal transferring circuit (Kusumoto et al. Col. 42 – 62).

Cited Reference

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The cited references relate to switches capacitor for Analog to Digital converter.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh Van Nguyen whose telephone number is (571) 272-1810. The examiner can normally be reached from 8:30 – 5:00 Monday-Friday. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Michael Tokar can be reached at (571) 272-1812. The fax phone numbers for the organization where this application or proceeding is assigned are (703-872-9306) for regular communications and (703-872-9306) for After Final communications.

Linh Van Nguyen

Art Unit 2819

09/08/04